BUFFERS, ISOLATION & PROTECTION OF OUTPUTS, and FAN-OUT

EGR/CS 333 Digital Design and Interfacing
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Adapted from some of my previous lecture notes, plus references:
http://www.electronics-tutorials.ws/logic/logic_9.html by Wayne Storr. Last updated: March 2011 **(MOST OF THIS HANDOUT)**
http://www.silabs.com/Support%20Documents/TechnicalDocs/an352.pdf by Silicon Labs

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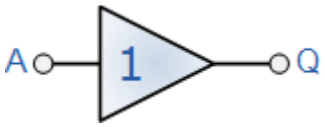
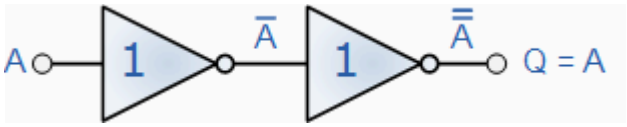
BUFFERS

A single input device that does noT invert or perform any logical operation on its input signal as its output exactly matches that of its input signal.

Symbol	Truth Table	
 **A Buffer**	A	Q
	0	0
	1	1
Boolean Expression **Q = A**	Read as **A** gives **Q**	

A Buffer can also be made by connecting together two NOT gates (Invertors):



You may think "what is the point of a Buffer if it doesn't alter its input signal in any way or make any logic decisions like the AND or OR gates, then why not use a piece of wire instead and that's a good point?

Buffers can be used **TO DRIVE HIGH CURRENT LOADS SUCH AS TRANSISTOR SWITCHES BECAUSE THEIR OUTPUT DRIVE CAPABILITY IS MUCH HIGHER THAN THEIR INPUT SIGNAL REQUIREMENTS, IN OTHER WORDS THEY HAVE A HIGH FAN-OUT CAPABILITY:**

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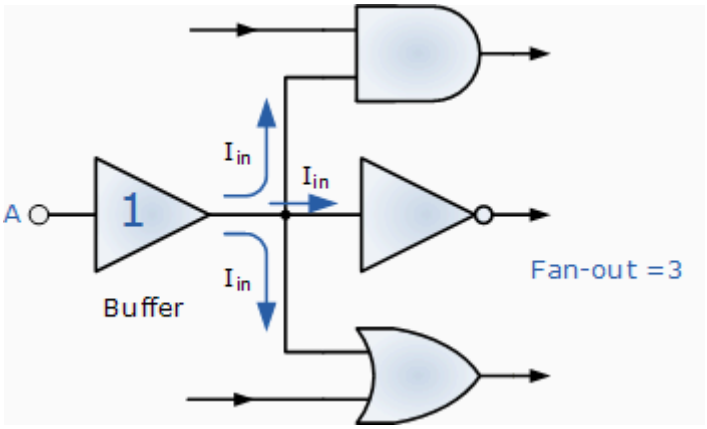


FAN-OUT is the output driving capability or output current capability of a logic gate. It may be necessary to connect more than one logic gate to the output of another or to switch a high current load such as an **LED**, then a Buffer will allow us to do just that by having a high fan-out rating of up to 50.

Buffers can be also be used to **ISOLATE** **OTHER GATES OR CIRCUITS FROM EACH OTHER**

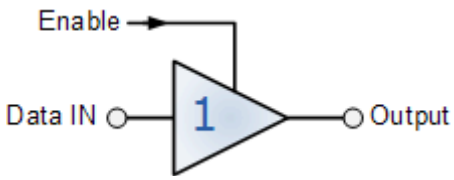
TRI-STATE BUFFER

A Buffer whose output can be "electronically" disconnected from its output circuitry when required; it can be thought of as an input controlled switch which has an output that can be electronically turned "ON" or "OFF" by means of an external "Control" or "Enable" signal input. This control signal can be either a logic "0" or a logic "1" type signal resulting in the Tri-state Buffer being in one state allowing its output to operate normally giving either a logic "0" or logic "1" output. **But when activated in the other state it disables or turns "OFF" its output producing an open circuit condition that is neither "High" or "low", but instead gives an output state of very high impedance, high-Z, or more commonly Hi-Z.**

This device has two logic state inputs, "0" or "1" but can produce three different output states, "0", "1" or "Hi-Z" which is why it is called a "3-state" device.

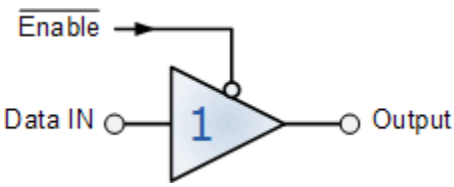
There are two different types of Tri-state Buffer, one whose output is controlled by an "**Active-HIGH**" control signal and the other by an "**Active-LOW**".

"ACTIVE-HIGH" Tri-state Buffer

Symbol	Truth Table		
 **Tri-state Buffer**	Enable	A	Q
	1	0	0
	1	1	1
	0	0	Hi-Z
	0	1	Hi-Z
Read as Output = Input if Enable is equal to "1"			

An **ACTIVE-HIGH** Tri-state Buffer is activated when a logic level "1" is applied to its "**enable**" control line and the data passes through from its input to its output. **When the enable control line is at logic level "0", the buffer output is disabled and a high impedance condition, Hi-Z is present on the output, PROVIDING GOOD ISOLATION TO PROTECT CIRCUITS BEING DRIVEN**

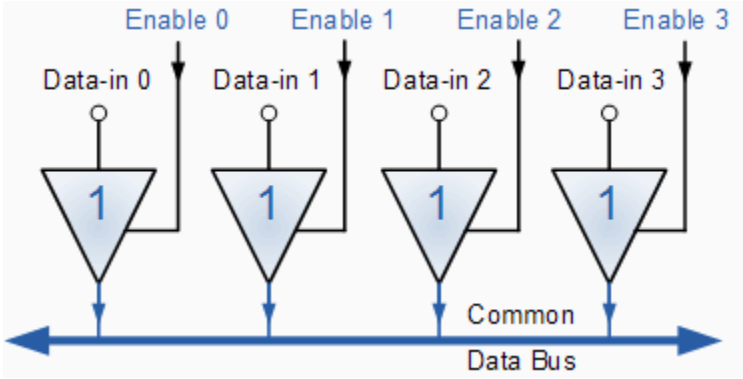
"ACTIVE-LOW" Tri-state Buffer

Symbol	Truth Table		
 **Tri-state Buffer**	Enable	A	Q
	0	0	0
	0	1	1
	1	0	Hi-Z
	1	1	Hi-Z
Read as Output = Input if Enable is **NOT** equal to "1"			

An **ACTIVE-LOW** Tri-state Buffer is activated when a logic level "0" is applied to its "**enable**" control line. The data passes through from its input to its output. **When the enable control line is at logic level "1", the buffer output is disabled and a high impedance condition, Hi-Z is present on the output, PROVIDING GOOD ISOLATION TO PROTECT CIRCUITS BEING DRIVEN**

Tri-state Buffer CONTROL

The Tri-state Buffer is used in many electronic and microprocessor circuits as they **ALLOW MULTIPLE LOGIC DEVICES TO BE CONNECTED TO THE SAME WIRE OR BUS WITHOUT DAMAGE OR LOSS OF DATA**. For example, suppose we have a data line or data bus with some memory, peripherals, I/O or a CPU connected to it. Each of these devices is capable of sending or receiving data onto this data bus. If these devices start to send or receive data at the same time a short circuit may occur when one device outputs to the bus a logic "1" the supply voltage, while another is set at logic level "0" or ground, resulting in a short circuit condition and possibly damage to the devices. The Tri-state Buffer can be used to isolate devices and circuits from the data bus and one another. If the outputs of several Tri-state Buffers are electrically connected together **Decoders** are used to allow only one Tri-state Buffer to be active at any one time while the other devices are in their high impedance state.



Commonly available **Digital Buffer** and **Tri-state Buffer** IC's include:

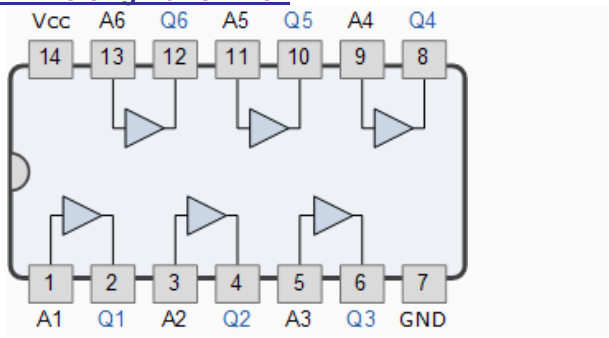
TTL Logic Types

- 74LS07 Hex Non-inverting Buffer
- 74LS17 Hex Buffer/Driver
- 74LS244 Octal Buffer/Line Driver
- 74LS245 Octal Bi-directional Buffer

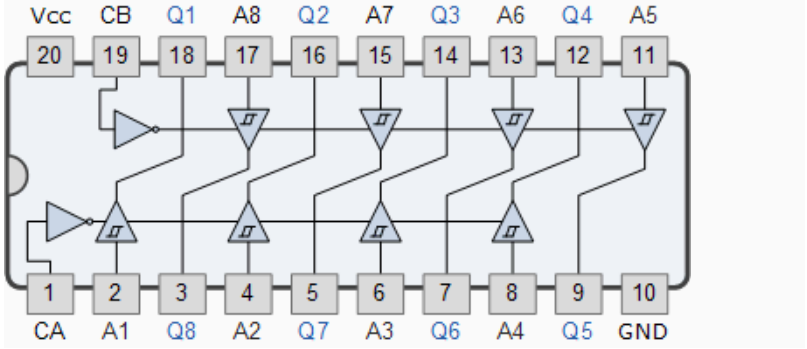
CMOS Logic Types

- CD4050 Hex Non-inverting Buffer
- CD4503 Hex Tri-state Buffer
- HEF40244 Octal Buffer with 3-state Output

Digital Non-inverting Buffer 7407



Octal Tri-state Buffer 74244



It is also possible to connect Tri-state Buffer "back-to-back" to produce a **Bi-directional Buffer** circuit with one "active-high buffer" connected in parallel but in reverse with one "active-low buffer". Here, the "enable" control input acts more like a directional control signal causing the data to be both read "from" and transmitted "to" the same data bus wire.

THE FOLLOWING IS JUST FOR REFERENCE IN EGR/CS333 :

More on isolation and design of bidirectional buses here:
http://www.silabs.com/Support%20Documents/TechnicalDocs/an352.pdf

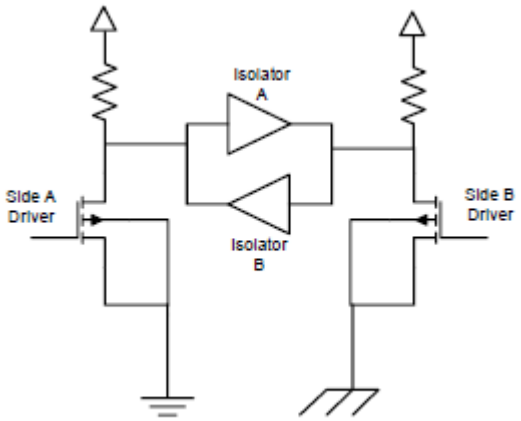


Figure 1.

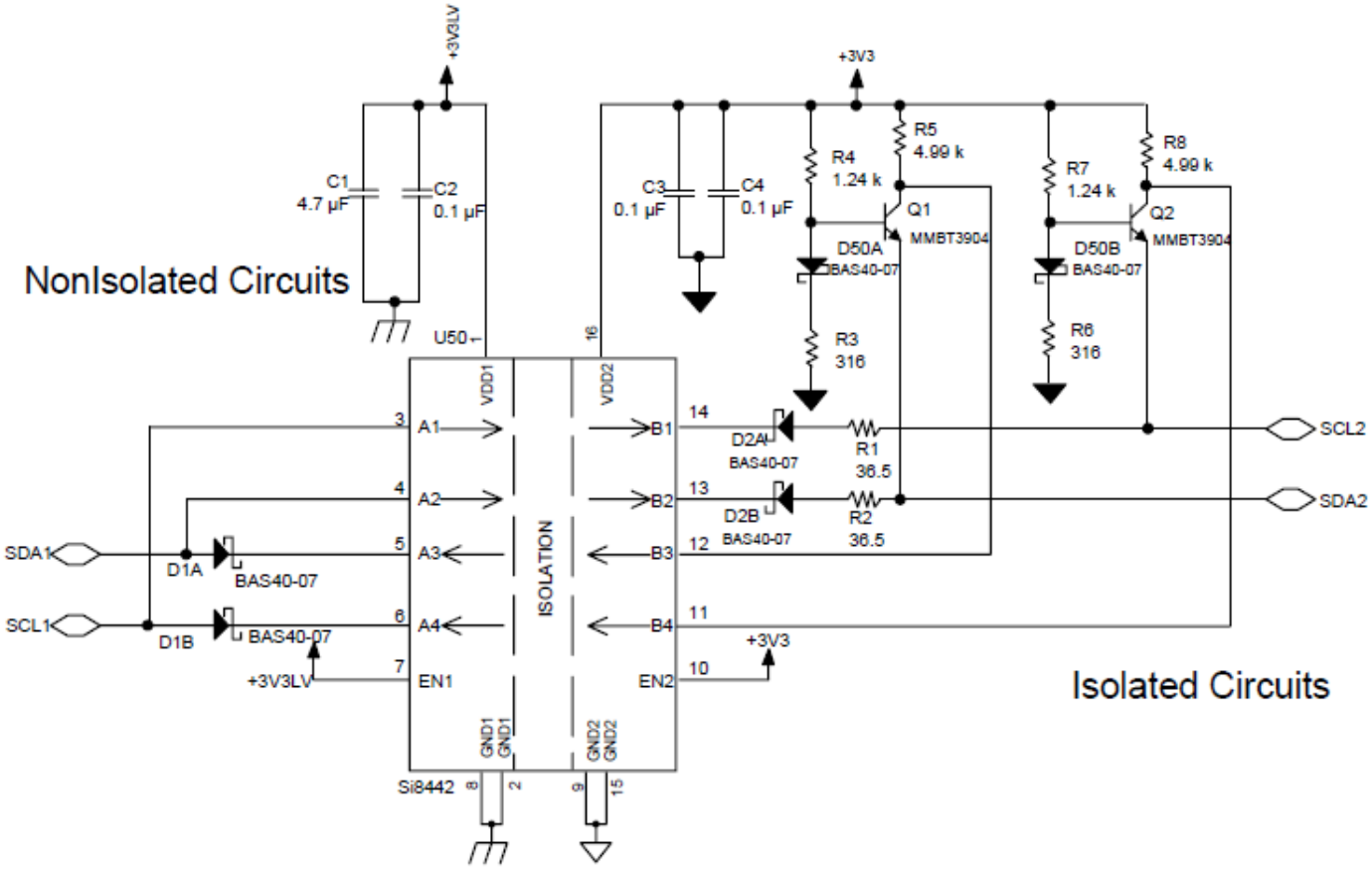


Figure 2. Full Circuit