



Vector/Array/Neuron Processor Design Plus Semester Highlights

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EGR 433: Advanced Computer Engineering
Elizabethtown College, Elizabethtown, PA

Processor Design Requirements:

Create 4 parallel scalar functional units with Vector Registers V_i , V_j , and V_k created from R_i 's, R_j 's and R_k 's of the 4 units. Use a 32-bit adder to add the two 16-bit product results from each unit. Put result into a 32 bit scalar accumulator, then into a neuron transfer function. Create an embedded code stack, controlled by a program counter via a master control unit with a Finite State Machine that implements the simple pipeline of Fetch, Decode, Execute, Write-Back, plus any special states. Embed a carefully crafted assembly language code segment to demonstrate the functionality of your instruction set.

Advanced PLC Highlight:

- Created Complex Voting Machine
 - Two Different Methods
 - Ladder Logic and Gates
 - Used in Industry, Aging Standard
 - Structured Text
 - High Level Programming Language
 - Global Variables Tied to I/O of Machine
 - LED's Triggered Based on Voting Criteria of Four Different Groups
 - Output LED's Also Triggered Based on Output Arithmetic
 - Versatility of \$5,000 Advanced PLC Controller

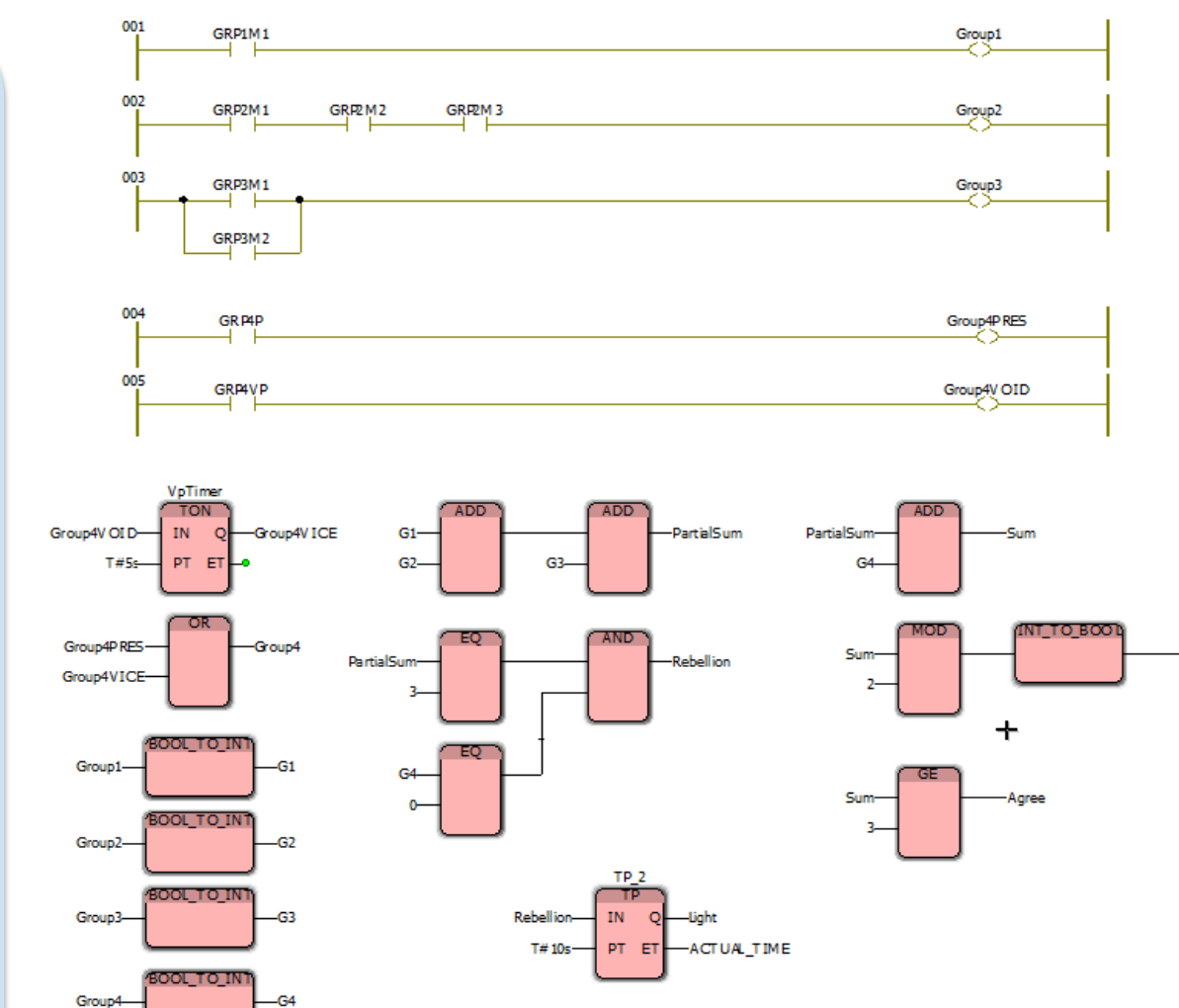


Figure 3: Ladder Logic and Gate Solution

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(* EGR433 Lab 7-8 PLC Program
Ryan Schick, Conor Csongradi, Lacie Flores *)
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Figure 4: Structured Text Solution Excerpt

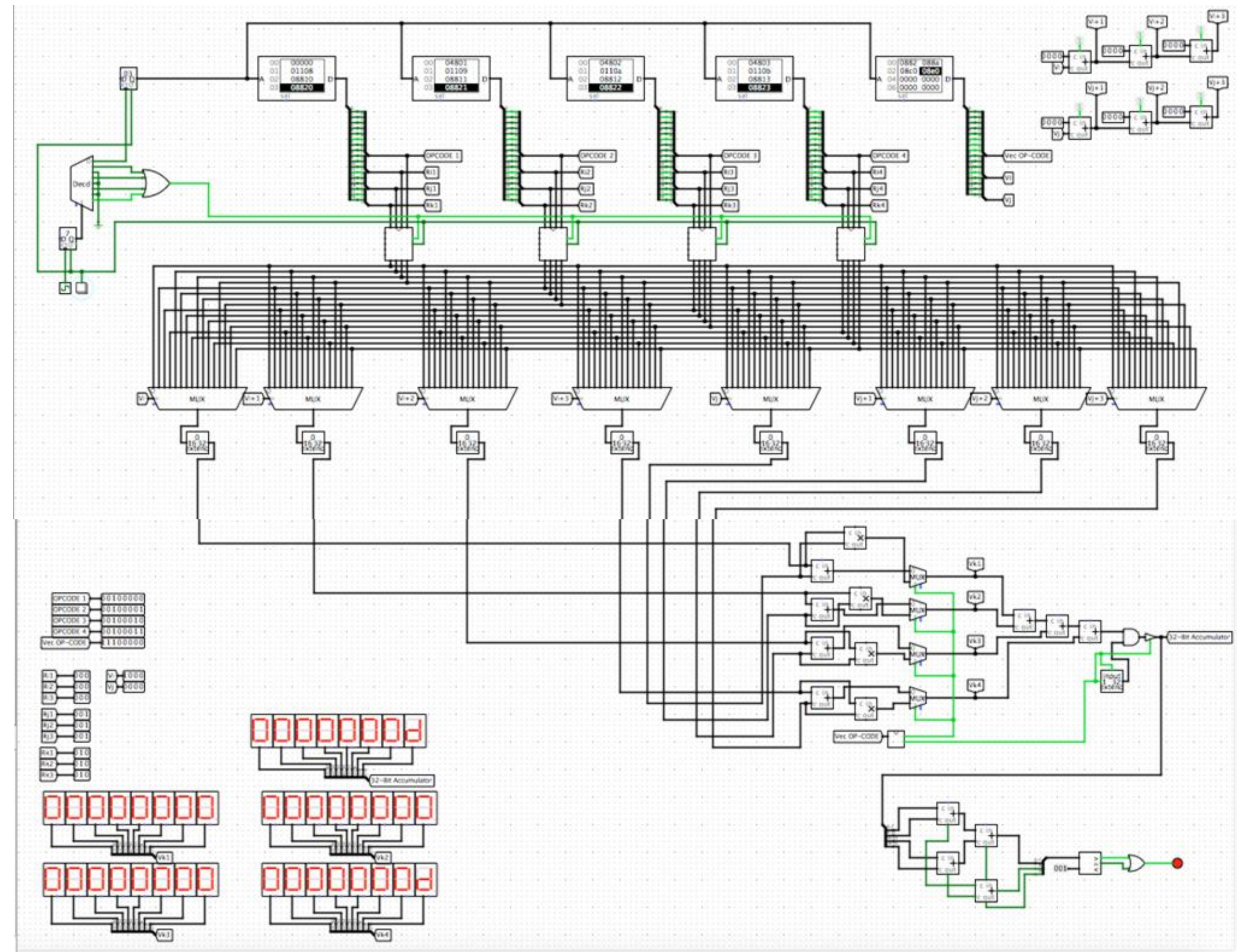


Figure 1: Vector/Array/Neuron Processor (Lab 7-8)

NanoLC Highlight:

- Implemented 2-Bit Up and Down Counters
 - Cycles Through all Possible Steps/Iterations
- Stores Counter Output in Registers
 - Comparator Designed Around Register Arithmetic
- Counter and Comparator Values Displayed via LED's
- Programmed via Flowchart Logic

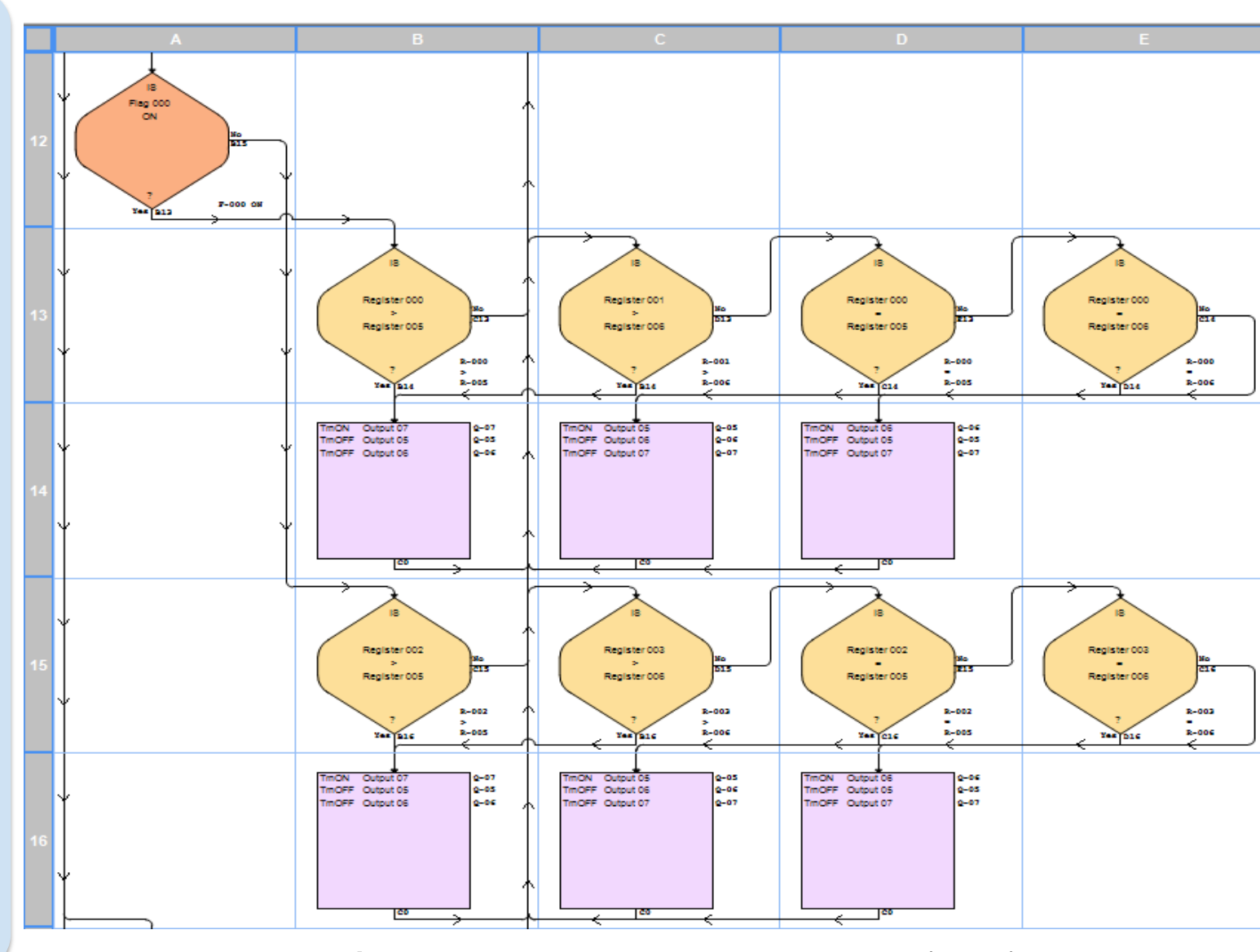


Figure 5: Flowchart Programming Excerpt (Lab 2)

FPGA/Xilinx Highlight:

- Created Digital Circuit Controlled By Four Bit Instruction Set
- Capable of 8-Bit Arithmetic
 - Stores Results in Registers
 - Outputs to Hex Display
- All 8-Bit Functional Blocks Created From Scratch

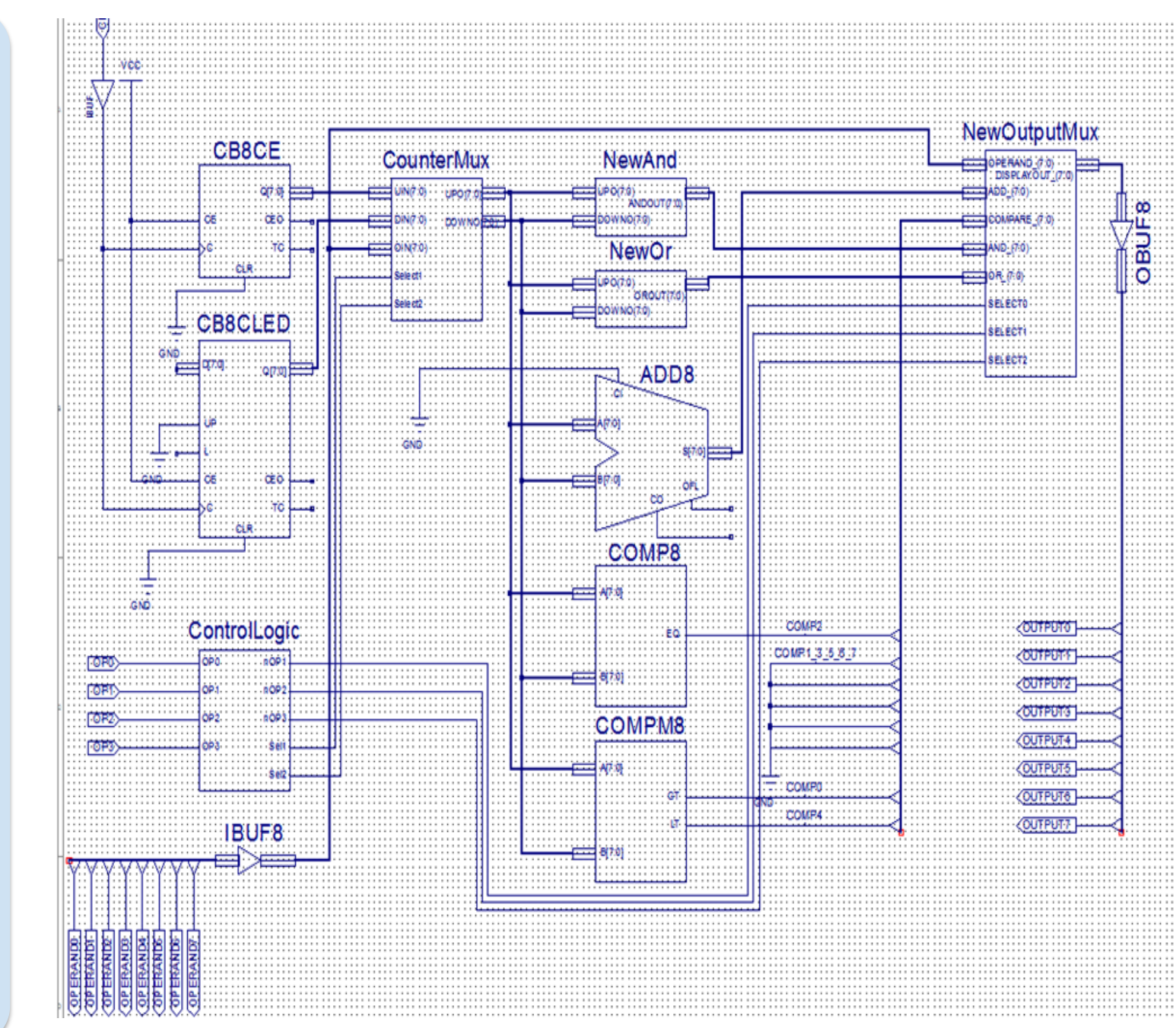


Figure 6: Digital Circuit Constructed in Xilinx (Lab 4)

Super Scalar Design Highlight:

Two parallel pipelines in a 2-way super scalar architecture. Uses a finite state machine that alternates between pipes.

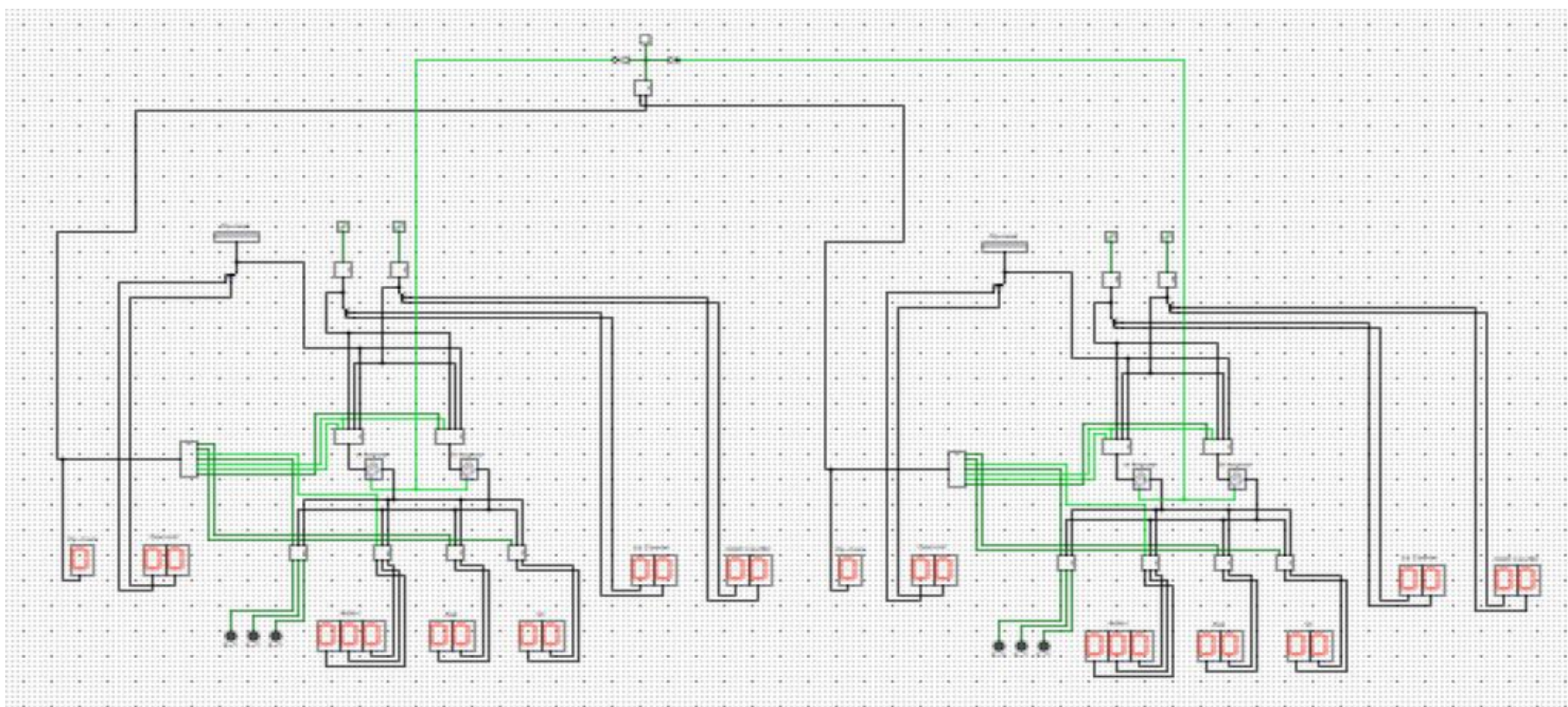


Figure 2: Super Scalar Digital Circuit (Lab 5)

Breadboarding/Power Supply Highlight:

- Modified an Old PSU to Serve as Power Supply for Breadboard Test Bench
- Stripped and Organized Wires According to ATX Layout
- Interfaced Testing Bench with NanoLC

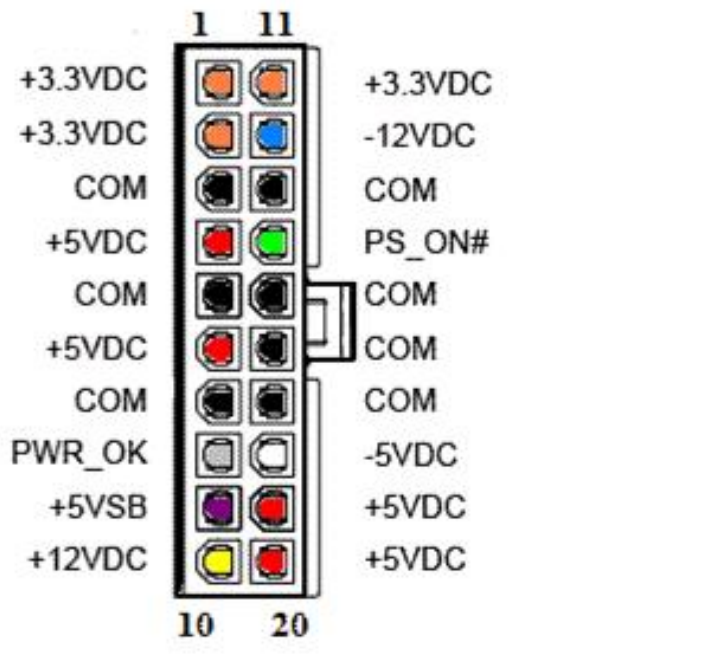


Figure 7: 20 Pin ATX PSU Pinout (Lab 4)