LS7166 Encoder to Microprocessor Interface Chip

Description:

The **LS7166** is an LSI monolithic CMOS building block useful in motion control applications. The 24-bit multi-mode counter register and logic enables a microprocessor to track the speed, direction, and position of an optical incremental shaft encoder. In addition to an 8-bit data bus, programmable realtime inputs and outputs are provided for hardware based control functions and status indication.

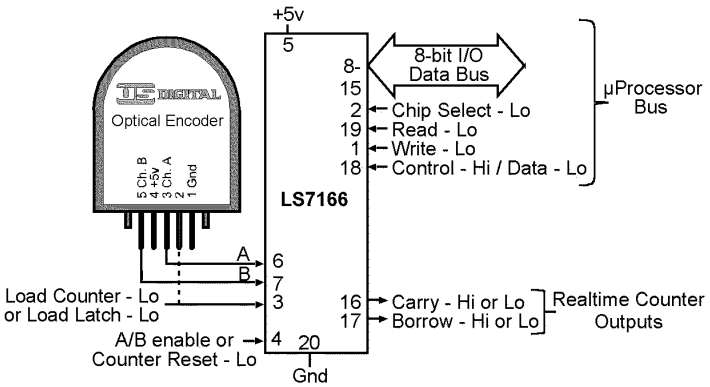
Note:
US Digital has already designed the ICs on this data sheet into various products. Please see the **PC7166**, **AD4-A** and **AD6** data sheets.

Features:

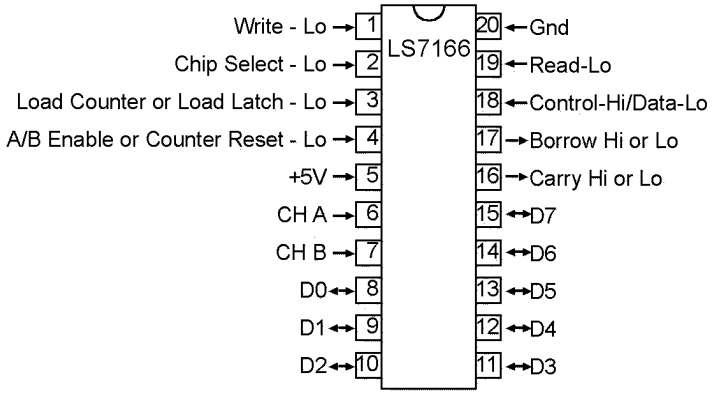
- X4 or X1 resolution multiplication.
- Preloadable 24-bit up/down counter.
- Choice of two 20-pin packages: SOIC surface mount or DIP (600mil).
- X1 or X2 or X4 resolution multiplier.
- Binary or BCD.
- Divide-by-N.
- 24-Bit comparator register.
- 4 control registers.
- Readable status register.
- 8-Bit tri-state I/O bus.
- DC to 10 MHz count frequency.
- Latched counter outputs.
- Input/output TTL & CMOS compatible.
- 5 volt operation.
- 200 uA supply current.
- No external clock required.

Absolute Maximum Ratings:

Parameter	Min.	Max.	Units
Operating temperature	0	70	℃
Storage temperature	-65	150	℃
Voltage at any input	-.5	VCC+.5	Volts
Supply voltage (VCC)		7	Volts

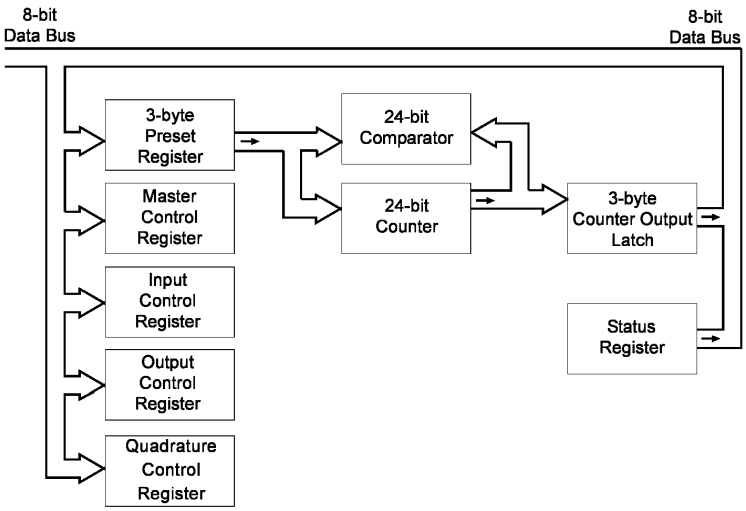


Example Circuit



Top View

Block Diagram of Counter & Registers:



Ordering Information:

	Price:
DIP Package (300mil):	
LS7166-DIP	$11.65 / 1
	$9.35 / 25
Surface Mount Package:	$7.45 / 100
LS7166-SOIC	$6.35 / 500
	$5.40 / 1k

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DC Electrical Characteristics:

Parameter	Min.	Max.	Units	Notes
Supply voltage	4.5	5.5	Volts	
Supply current	-	200	µA	@ 5.0V
Input low voltage	-	0.8	Volts	
Input high voltage	2.0	-	Volts	
Output low voltage	-	0.4	Volts	@4mA sink
Output high voltage	2.5	-	Volts	@200µA source
Input current	-	15	nA	leakage current
Output source current	200	-	µA	@V_{OH} = 2.5V
Output sink current	4	-	mA	@V_{OL} = 0.4V
Data bus off-state				
Leakage current	-	15	nA	

Realtime Hardware Input Pin Descriptions:

A & B (Inputs) (Pins 6 & 7):
Connect to A & B quadrature outputs of the encoder. The quadrature code will be decoded and used to clock and steer the 24-bit Counter. It can be programmed to generate one clock once per quadrature cycle, once per 1/2 cycle or once per 1/4th cycle (X1, X2 or X4 mode). Maximum count frequency is 10 MHz.

A/B Enable or Counter Reset (Input) (Pin 4):
Active low. Minimum low pulse width is 60ns. The function of this pin is defined by bit-4 of the Input Control Register. When bit-4 is low, a low level on this pin will reset the 24-bit counter. When bit-4 is high, a low level on this pin will enable the A & B inputs.

Load Counter or Load Latch (Input) (Pin 3):
Active low. Minimum low pulse width is 60ns. The function of this pin is defined by bit-5 of the Input Control Register. When bit-5 is low, a low level on this pin will transfer the contents of the 24-bit Preset Register to the 24-bit Counter. When bit-5 is high, a low level on this pin will transfer the contents of the 24-bit Counter to the 24-bit Counter Output Latch.

Microprocessor Bus Pin Descriptions:

Data Bus (Pins 8-15):
Three-state, 8-bits. Used to pass data to and from the internal registers in single and multiple-byte transfers. Bits 6 & 7 are used as address bits to select the desired control registers during write operations.
Chip Select (Input) (Pin 2):
Active Low, enables the chip to Read or Write on the data bus.
Read (Input) (Pin 19):
Active Low, enables the Status Register or 1-byte of the 24-bit Output Latch to be read on the data bus.
Write (Input) (Pin 1):
Active Low, during chip select, latches the data bus into the internal registers.
Control-Hi/Data-Lo (Input) (Pin 18):
Used to address various resistors during read and write cycles. A high level during a read cycle selects the Status Register. A high level during a write cycle selects 1 of the 4 Control Registers. A low level during a write cycle selects one byte of the Preset Register. A low level during a read cycle selects one byte of the Counter Output Latch.

Output Control Register (Write only):

4 useful bits. Initializes the 24-bit Counter and sets operating modes. Select this register by making bit-6 low and bit-7 high. Control functions may be combined.
Bit-0: Low level selects binary count mode. High level selects BCD count mode.
Bit-1: This bit must be reset low for normal operation.
Bit-2: Low level selects normal wrap-around count mode. High level selects divide-by-N mode (24-bit counter is reloaded from the Preset Register upon Carry or Borrow).
Bit-3: This bit must be reset low for normal operation.
Bits 4 & 5: The functions of hardware pins 16 & 17 are defined by these two bits. Pin 16 can be defined as any of the following:

Bit-5	Bit-4	Pin 16 Function
0	0	Carry - low true
0	1	Carry toggle flip flop (starts out low)
1	0	Carry - high true
1	1	24-bit Comparator/Counter match - low true

Pin 17 is also defined the the same two bits as follows:

Bit-5	Bit-4	Pin 17 Function
0	0	Borrow - low true
0	1	Borrow toggle flip flop (starts out low)
1	0	Borrow - high true
1	1	24-bit Comparator/Counter match - high true

Readtime Hardware Output Pin Description:

Carry or Match (Output) (Pin 16):
The function of this pin is defined by bits 4 and 5 of the Output Control Register as follows:

Bit-5	Bit-4	Pin Function
0	0	Carry - low true
0	1	Carry toggle flip flop (starts out low)
1	0	Carry - high true
1	1	24-bit Comparator / Counter match - low true

Borrow or Match (Output) (Pin 17):
The function of this pin is also defined by bits 4 and 5 of the Output Control Register as follows:

Bit-5	Bit-4	Pin Function
0	0	Borrow - low true
0	1	Borrow toggle flip flop (starts out low)
1	0	Borrow - high true
1	1	24-bit Comparator/Counter match - high true

Note that the functions of pins 16 and 17 are defined by the same 2 bits of the Output Control Register. They are inseparably linked together.
The toggle flip flops are triggered by the trailing edges of the associated Carry, Borrow, or Compare match. Thus there is a 1-clock delay between the input and output of each flip flop.
Unless otherwise specified, assume the longest prop delay from any input to any output is <110ns.

Status Register (Read only, Control):

Bits 5, 6 and 7 are always high.
Bit-0: Borrow Toggle Flip-Flip. Toggles every time the 24-bit counter underflows generating a borrow.
Bit-1: Carry Toggle Flip-Flip. Toggles every time the 24-bit counter overflows generating a carry. Trailing edge triggered.
Bit-2: Compare Toggle Flip Flop. Toggles every time the 24-bit counter equals the 24-bit Preset Register. Trailing edge triggered.
Bit-3: Sign bit. Set low when a Borrow occurs. Set high when a Carry occurs. Level triggered.
Bit-4: Up/Down Counter Direction. Reset low when counting down, Set high when counting up. Leading edge triggered.
Bits 5, 6 and 7 are always high.

Register Access:

Writing to 1 of the 4 Control Registers: Set Control/Data high. Bits 6 & 7 are used as address bits to select one of these 4 registers. Only bits 0-5 are stored.

D7	D6	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
X	X	X	X	X	1	Disable Chip for Read or Write
0	0	1	1	⌐⌐	0	Write to Master Control Register
0	1	1	1	⌐⌐	0	Write to Input Control Register
1	0	1	1	⌐⌐	0	Write to Output Control Register
1	1	1	1	⌐⌐	0	Write to Quadrature Control Register
X	X	0	1	⌐⌐	0	Write to Preset Register, then increment Address Counter
X	X	0	⌐⌐	1	0	Read Output Latch, then increment Address Counter
X	X	1	⌐⌐	1	0	Read Output Status Register

Notes:
D7 & D6 are the Most significant bits of the data bus.
C/D is Control/Data pin 18. RD is Read pin 19. WR is Write pin 1. CS is Chip Select pin 2. X means "don't care".
Write Cycle Timing: Allow at least 15ns setup time for valid data, Chip Select and Control/Data before asserting Write. Make the write pulse at least 60ns long. Hold the data bus, Chip Select and Control/Data stable at least 50ns after deasserting Write.
Read Cycle Timing: The data bus will become valid within 110ns after asserting Chip Select, Control/Data and Read.

Preset Register (Write only, Data):

The 24-bit Preset Register is the input port for the 24-bit counter. The data is first written into the Preset Register in 3 write cycles (least significant byte 1st). The address pointer is automatically incremented with each write cycle.

Sequence:
• Reset the address pointer by setting bit-0 of the Master Control Register high.
• Load byte 0 (LSB) into this register & increment address
• Load byte 1 into this register & increment address
• Load byte 2 (MSB) into this register & increment address
• Transfer the 3-byte Preset Register to the 24-bit counter by setting bit-3 high of the Master Control Register.

Input Control Register (Write only):

Defines the operating mode of this chip. Select this register by making bit-6 high and bit-7 low.
Bits 0, 1 & 2: These bits must be reset low for normal operation.
Bit-3: Reset low to disable the A & B inputs. Set high to enable the A & B inputs.
Bit-4: The function of hardware pin 4 is defined by this bit. When bit-4 is low, a low level on pin 4 will reset the 24-bit counter. When bit-4 is high, a high level on pin 4 will disable the A & B inputs.
Bit-5: The function of hardware pin 3 is defined by this bit. When bit-5 is low, a low level on pin 3 will transfer the contents of the 24-bit Preset Register to the 24-bit Counter.
When bit-5 is high, a low level on pin 3 will transfer to contents of the 24-bit Counter to the 24-bit Counter Output Latch.

Master Control Register (Write only):

Performs register reset and load operations. Select this register by making bits 6 and 7 low. Writing a non-zero byte to this register does not require a follow-up write of an all-zeros byte to terminate an operation. Control functions may be combined.
All bits are high true.
Bit-0: Reset the 3-byte Address Pointer, in preparation for a 3-byte (24-bit) write sequence of the Preset Register or read sequence of the Output Latch.
Bit-1: Transfer the 24-bit Counter contents to the 24-bit Output Latch.
Bit-2: Reset the 24-bit Counter, the Borrow Toggle Flip-Flop and the Carry Toggle Flip-Flop and set the Sign bit high.
Bit-3: Transfer the 24-bit Preset Register to the 24-bit Counter.
Bit-4: Reset the Comparator Match Toggle Flip-Flop.
Bit-5: Master Reset. Reset the 24-bit Counter, the Input Control Register, the Output Control Register, the Quadrature Register, the Borrow Toggle Flip-Flop, the Carry Toggle Flip-Flop, the Comparator Toggle Flip-Flop and the 3-byte address pointer. Note: Master reset does not reset the counter perfectly. The counter will be either 1, 0 or -1 after a master reset. To reliably reset the counter to 0, do a Reset Counter Command with bit-2 as shown above.

Counter Output Latch (Read only, Data):

The 24-bit counter value at any instant can be accessed by transferring its contents to the 24-bit Counter Output Latch. Note that only good stable data will be passed from the counter to the Output Latch even if the counter bits are in the midst of a transition. This chip will internally stretch the latch pulse if necessary until the counter has stabilized. The 3 bytes are then read from the Output Latch (least significant byte 1st). The address pointer is automatically incremented with each read cycle.

Sequence:
• Reset the Address Pointer and transfer the Counter value to the Output Latch by setting bits 0 and 1 of the Master Control Register high. These bits will automatically reset to zero after the Read Sequence.
• Read byte 0 (LSB) and increment address
• Read byte 1 and increment address
• Read byte 2 (MSB) and increment address

Quadrature Control Register (Write only):

Selects the quadrature count mode. Select this register by making bit-6 high and bit-7 high. It can be programmed to generate one clock once per quadrature cycle, once per 1/2 cycle or once per 1/4th cycle (X1, X2 or X4 mode). For example, a 500 cycle/rev encoder can provide 500, 1000 or 2000 counts/rev.
Bits-0 & 1:

Bit-1	Bit-0	Quadrature Count Mode
0	0	Not valid
0	1	X1 mode
1	0	X2 mode
1	1	X4 mode

Bits-3 & 5: These bits do not matter.