#### Elizabethtown College Syllabus "Digital Design II, Assembly Language, and Interfacing" EGR/CS 333

#### Spring, 2021

Advanced digital logic design and circuit implementations. Assembly language programming. Design, testing, and construction of interfaces, and design and testing of supporting software. Programmable Logic Controllers (PLC's), Microcontroller development systems. Breadboarded TTL circuit implementations. Circuit simulators. Raspberry pi's, Arduino's, and similar simple devices. Intro to Field

Programmable Gate Arrays (FPGA's). Custom lab manuals. Introductory Robotics projects.

\*Prerequisite(s): CS332/EGR332, Hours: lecture 3, laboratory 3. Spring semester, odd-numbered years.

Professor: Joseph T Wunderlich PhD, Associate Professor of Engineering and Computer Science

Offices: E284E, and E273, however just virtual this semester Office: 717-361-1295 Cell: 717-368-9715 Email: wunderjt@etown.edu Website: http://users.etown.edu/w/wunderjt Office Hours & Calendar: http://users.etown.edu/w/wunderjt/schedules/CALENDAR3\_s21\_web.htm

## Course Credit: 4

Contact Hours: 6 (therefore 6 x 50 = 300 minutes per week of "contact"); Typical weekly distribution:

- 120 minutes of Lecture
- 120 minutes of Lab
- 60 minutes of Studio for combined lecture/lab/presentations/etc.

## **Meeting Times**

We meet 300 minutes per week (as expected for 6 contact-hours);

Mondays 12:30-2:20 (110 minutes) REMOTE – via zoom links in Canvas

Wednesdays 12:30-3:10 (160 minutes) in E273 - also optional via zoom links in Canvas

- Invited Speakers (30 minute/week average to total remaining minutes). Locations and times to be announced
  - 1. Friday Feb 12@ 7:00pm U.S. Submarine Officer Alex Wunderlich, BS Mechanical and Nuclear Engineering at Virginia Tech, M.S. Naval Architecture (in progress) at M.I.T.
  - 2. Tuesday Feb 23 @ 3:00pm Virtual Company Meet & Greet
  - 3. Guest Lecture by U.S. Ambassador John B Craig on U.S. National Security Policy
  - 4. Cybersecurity Symposium
  - 5. TBA

### Course Objectives

- 1. Hardware and software design for interfacing
- 2. Assembly language programming
- 3. Advanced digital circuit design
- 4. Breadboard circuit implementations
- 5. Programmable Logic Controllers (PLC's) implementations
- 6. Field Programmable Gate Arrays, Raspberry Pi's, Arduino's, etc.
- 7. Simulation Software Engineering vs. Real-time Code Development

### Prerequisite Topics

- 1. Intermediate programming skills (from CS122)
- Introduction to assembly language programming (from EGR/CS332)
- 3. Computer architecture (register-transfer level data-flow), (from EGR/CS332)
- Computer architecture (register italiser lover data low), (*irom EGR/CS332*)
   Computer architecture (gate-level data-flow and control), (*from EGR/CS332*)
- Combinational digital circuit design, (from EGR/CS332)
- Sequential digital circuit design, (*from EGR/CS332*)

## Grading

- 50% 60% 70% (700 points) Laboratory projects
- 20% (200 points) Midterm exam(s)
- 30% 20% 10% (100 points) Comprehensive Final Exam
  - COURSE GRADE:

(60-62)=D-, (63-67)=D, (68-69)=D+, (70-72)=C-, (73-77)=C, (78-79)=C+, (80-82)=B-, (83-87)=B, (88-89)=B+, (90-92)=A-, (93-100)=A (with any fractional part rounded to the nearest integer)

## Course Texts, Manuals, and Readings excerpts from below will be included or handed out in class

- Frank D. Petruzella, "Programmable Logical Controllers," 4th edition, September 3, 2010, McGraw-Hill Science/Engineering/Math, (ISBN: 0073510882).
   Arijit Saha and Nilotoal Manna. "Digital Principles and Logic Design." 1st edition. January 28, 2009. Jones & Bartlett Publishers. (ISBN: 978076377373).
- Arijit Saha and Nilotpal Manna, "Digital Principles and Logic Design," 1st edition, January 28, 2009, Jones & Bartlett Publishers, (ISBN: 978076377373). This is the text used for prerequisite course EGR/CS332
- 3. Kenneth Ayala, "8051 Microcontroller: Architecture, Programming and Applications," 2 edition, September 26, <u>1996</u> this one is much better than the newer editions), Delmar Learning, (ISBN: 9780314201881).
- 4. ETOWN: 2018 IC's, Circuit Trainer, and Power Supply Manual
- 5. ETOWN: 2019 FPGA Board & Xilinx software Manual (previous versions: 2018b 2018a, 2013, pre-2013)
- 6. ETOWN: 2019 Phoenix Contact NanoLC Programmable Logic Controller Manual (previous version:2018)
- 7. ETOWN: 2019 Phoenix Contact AXL/AXC PLC Manual (previous versions: 2018, 2017)
- 8. ETOWN: 2019 Raspberry Pi and ARM Microcontroller Assembly Language Manual and Labs (previous version: 2017)
- 9. ETOWN: 2019 Intel 80251 Microcontroller Assembly Language Manual (previous versions: 2015, 2014, pre-2013)
- 10. ETOWN: 2019 Relays Manual

Attendance Policy:

## Do not come to class sick! (Else minus variable points depending on severity of illness)

## Course Outline

- ADVANCED COMBINATIONAL & SEQUENTIAL LOGIC DESIGN, and BREADBOARDING
  - O Review of mandatory-prerequisite course material from EGR/CS332 Digital Design I: 332 review #1
    - O Fan-out, Floating pins, Pull-up resistors
      - Resistors: part 1 part 2
    - o Debouncing Switches
      - waveform analysis 1 waveform analysis 2
      - BiPolar vs. CMOS transistor technology & Integrated Circuits
      - LAB-MANUAL & TUTORIAL: 2018 IC's, Circuit Trainer, and Power Supply
    - Logisim circuit simulator
- ISOLATION

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- Relays(video)
- o "Relays" Guest Lecture by Arnold Offner (Phoenix Contact)
- o LAB-MANUAL & TUTORIAL: 2019 Relays
- o Buffers
- MOTORS
  - o DC Motors
  - o AC
  - o AC&DC Motors
- SENSOR FUSION & REAL-TIME CONTROL (e.g., for ROBOTICS)
  - Robotics Sensors and Navigation
  - Programmable Logic Controllers (PLC's)
    - Ladder Logic
    - PLC's
    - Fundamentals
    - Evolution
  - LAB-MANUAL & TUTORIAL: 2019 NanoLC (Phoenix Contact)
  - o LAB-MANUAL & TUTORIAL: 2019 Advanced PLC (Phoenix Contact)
  - 2021 Advanced PLC (Phoenix Contact "PLCnext")
- COMMUNICATIONS
  - O Part 1
  - O Part 2
- SIMULATIONS vs. REAL-TIME CONTROL
  - O Dr W's 1990 Sim vs Real-Time Control of a Bottling Plant
  - o Dr W's 2001 ASEE: "Simulation vs. Real-Time control; with Application to Robotics and Neural Networks" Talk
  - o AI & Neural Networks Intro
  - o Dr W's 2002 IEEE: "Development of an Interactive Simulation with Real-time Robots for Search and Rescue"
- MICROCOLLERS and ASSEMBLY LANGUAGE PROGRAMMING
  - o Dr W's 1999 ASEE: "Focusing on Blurry Distinction between Microprocessors and Microcontrollers" 332 review #2
  - Intel 8051 Microcontroller:
  - o Overview (pin-out, architecture, etc)
  - o Memory Map
  - o **PSW**
  - o Stack
  - Instruction Set (1,2)
    - MOVES
    - LOGIC
    - MATH
    - JUMPS&CALLS (PPT,text)
    - 80251
  - o LAB-MANUAL & TUTORIAL: 2019 Intel 8051 Microcontroller (2015, 2014, Pre-2013)
    - LAB-MANUAL & TUTORIAL: 2019 Raspberry Pi and ARM Microcontroller
      - ARM Assembly Language Programming
- ROBOTICS CASE STUDIES

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- FIELD PROGRAMMABLE GATE ARRAYS (FPGA'S) this is mostly for EGR433 "Advanced Computer Engineering"
  - o LAB-MANUAL & TUTORIAL: 2019 FPGA (2018B, 2018A, 2013, pre-2013)

## LABS

## SPECIAL FEES DURING COVID: Although all parts and equipment are usually supplied in the laboratory, student may be required to purchase up to \$200 of parts/devices to accommodate working out of the lab during Covid

IF LABS ARE BUILT (AND POSSIBLY REBUILT), BUT DON'T FULLY FUNCTION: For demonstrations and reports, deduct depends on how adequately you identify problems. For example, make test set-ups to verify functionality of isolated simulation sub-parts, chips, circuit trainer elements, software, relays, other electronics, motors or other higher-voltage circuits and devices. PROVE THAT NO EASY FIX OR SUBSTITUTION WAS POSSIBLE or EASILY IDENTIFIABLE AT THE TIME. Discuss (1) How you identified problems, and (2) How you tried to fix them. Include evidence that you fully understand and have properly connected all pins on a given chip (including considering floating-pins, powering the chip, needed pull-up resistors, proper voltage levels, etc.), and that you have exhausted much time attempted to solve all problems).

### **REPORTS** must include:

- PHOTO'S OF ALL CIRCUITS (AND TEST-SET-UP'S BUILT)
- Title Page with lab number, name of lab, your names, Majors, Year (e.g., Junior), who is demonstrating, and who is the designated TEAM LEADER
- Sections numbered and tilted as follows (always list all of these, and simply put "NA" if not applicable):
  - "Assignment" (An exact copy of everything in this document -- exactly how it looks here)
  - "Equipment Used" (A list of hardware and software) INCLUDE PHOTO'S OF ALL EQUIPMENT 2
  - "Methodology" (including all design steps, analysis, DECISIONS MADE, etc.) INCLUDE PHOTO'S OF ALL CIRCUITS BUILT 3
  - 4 "Options" (if applicable, a comparison of each method used)
  - "Problems Encountered" (including any debugging methodology) INCLUDE PHOTO'S OF ANY TEST-CIRCUITS BUILT 5.
  - "Testing Methodology" (including timing traces, test-vectors, and RATIONALE FOR HOW YOUR METHODOLOGY ASSURES QUALITY) including 6. estimated probability of satisfactory coverage by chosen test vectors
  - 7. "References" (in standard IEEE format)
  - "Appendices" (for spec sheets, etc.)
- ALL DESIGN PROCESS STEPS MUST BE INCLUDED for Digital Logic designs (NUMBERED as in EGR/CS 332). If design step not done, list as "N.A." For Combinational Digital Logic Design:
  - - Step 1: Define problem
    - Step 2: Encode variables Step 3: Create truth table
    - Step 4: Find simplified function(s)
    - Step 5: Draw logic circuit
    - Step 6: Convert to NAND's
    - Step 7: Check assumptions
    - Step 8: Chip circuit diagram
  - For Sequential Digital Logic Design::
  - Step 1: Define problem
  - Step 2: Create state diagram
  - Step 3: Encode variables
  - Step 4: Minimize machine
  - Step 5: Create state table
  - Step 6: Append flip-flop inputs
  - Step 7: Find simplified function(s)
  - Step 8: Draw logic circuit
  - Step 9: Convert to NAND's
  - Step 10: Analyze any unused states
  - Step 11: Revise state diagram
  - Step 12: Check Assumptions
  - Step 13: Chip circuit diagram
  - COLOR-CODED LOGIC DIAGRAMS are required for any digital circuit (Breadboard, FPGA, etc.)
- COLOR-CODED CIRCUIT SCHEMATICS are required for any circuit implemented (Breadboard, PLC, ladder logic, etc.), color is a must, hand-colored is ok .
- FLOW CHART is required for any program
- COMMENT EVERY LINE OF CODE
- TEAM LEADER has responsibility of coordinating all equipment problems and acquisition of needed parts. Try to stick with same person for this role.

#### DEMONSTRATIONS

Alternate team members demonstrate lab to me (partners must be present). We do this for previous week's assignment while you begin the next assignment

GRADING for both demonstrations and reports, a 92 is for everything done very well and professional; to get more points, enhance things in creative way

## Disabilities

Elizabethtown College welcomes otherwise qualified students with disabilities to participate in all of its courses, programs, services, and activities. If you have a documented disability and would like to request accommodations in order to access course material, activities, or requirements, please contact the Director of Disability Services, Lynne Davies, by phone (361-1227) or e-mail daviesl@etown.edu. If your documentation meets the college's documentation guidelines, you will be given a letter from Disability Services for each of your professors. Students experiencing certain documented temporary conditions, such as post-concussive symptoms, may also gualify for temporary academic accommodations and adjustments. As early as possible in the semester, set up an appointment to meet with me, the instructor, to discuss the academic adjustments specified in your accommodations letter as they pertain to my class.

# Learning Outcomes

Yellow / Highlighted = Graded student works collected in Binders for internal & external-ABET review				Prog	ram C	oordi	nator	
2018/19 New ABET Learning Outcomes An ability to:	Imati		ioo					
(ABET-1) Identify, formulate, and <u>solve</u> complex engineering problems by applying principles of engineering, science, and (ABET-2) Apply engineering <b>design</b> to produce solutions that meet specified needs with consideration of public health, sat				95 W4	all as	aloha	1	
cultural, social, environmental, and economic factors.	oty, a		Jilaro,	a5 w	11 45	gioba	",	
(ABET-3) Communicate effectively with a range of audiences.								
(ABET-4) Recognize ethical and professional responsibilities in engineering situations and make informed judgments, which	h mu	st cor	sider	the				
impact of engineering solutions in global, economic, environmental, and societal contexts.								
(ABET-5) Function effectively on a team whose members together provide leadership, create a collaborative and inclusive	env	ronm	ent, e	stablis	ih goa	als,		
plan tasks, and meet objectives.	-			- (1.4)				
(ABET-6) Develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to (ABET-7) Acquire and apply new knowledge as needed, using appropriate learning strategies.	draw	conc	lusion	IS ( <u>LA</u>	<u>o s</u> ).			
(Her T) require and appy non-knowedge as needed, along appropriate rearring endogree.								
Pre-2018/19 ABET Learning Outcomes								
(ABET-a): An ability to apply knowledge of mathematics, science, and engineering.								
(ABET-b): An ability to design and construct experiments, as well as to analyze and interpret data.								
(ABET-c): An ability to design a system, component, or process to meet desired needs.								
(ABET-d): An ability to function on multi-disciplinary teams if possible, or to draw on the talents of others					_	_		
(ABET-e): Identify, formulate, and solve engineering problems (ABET-f): An understanding of professional and ethical responsibility						_		
(ABET-g): Communicate effectively orally and in writing								
(ABET-h): A broad education necessary to understand the impact of engineering solutions in a global and	soci	etal	conte	ext				
(ABET-i): Recognition of the need for, and an ability to engage in life-long learning								
(ABET-j): Knowledge of contemporary issues								
(ABET-k): An ability to use the techniques, skills, and modern engineering tools necessary for engineering	pra	ctice			_	_		
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M = Medium Emphasis in Course	ğ		ica	Ĕ	¥		arr	
L = Low or no Emphasis in Course	Solve Problems	c	Communication	Ethics & Impacts	Teamwork		How to learn	
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2018/19 New ABET Learning Outcomes:	1	2	3	4	5	6	7	CREDITS
Pre-2018/19 ABET Learning Outcomes:	•	_	g	fhj	d	bk	i	REC
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Class Cancelation Any non-emergency class cancelation will be announced via email at least a two hours before class time, in addition to signage posted by Department Administrative Assistants. Any makeup work will be announced to insure all intended course content is covered.

## **Religious Observations**

The College is willing to accommodate individual religious beliefs and practices. It is your responsibility to meet with the class instructor in advance to request accommodation related to your religious observances that may conflict with this class, and to make appropriate plans to make up any missed work

## Academic Honesty

Elizabethtown College Pledge of Integrity: "Elizabethtown College is a community engaged in a living and learning experience, the foundation of which is mutual trust and respect. Therefore, we will strive to behave toward one another with respect for the rights of others, and we promise to represent as our work only that which is indeed our own, refraining from all forms of lying, plagiarizing, and cheating." See the 2016-17 Elizabethtown College Catalog, "Standards of Academic Integrity" (Academic Integrity) at Elizabethtown College, 11th ed. (https://www.etown.edu/offices/dean-of-students/files/academic-integrity-handbook.pdf).